REPORT DOCUMENTATION PA

1 AGENCY USE ONLY (Leave blank)	2 REPORT DATE	3 REPORT TYPE AND DATES COVERED
	October 1993	Viewgraphs

4 TITLE AND SUBTITLE
GENERALIZED EMULATION MICROCIRCUIT PROGRAM

5 FUNDING NUMBERS
PR: EE78
PE: DBOF
WU: DN388541

6 AUTHOR(S)
H. Hanson, J. Christensen

7 PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Command, Control and Ocean Surveillance Center (NCCOSC)
RDT&E Division
San Diego, CA 92152-5001

8 PERFORMING ORGANIZATION REPORT NUMBER

9 SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Defense Logistic Agency
Cameron Station
Alexandria, VA 22304-6100

10 SPONSORING/MONITORING AGENCY REPORT NUMBER

11 SUPPLEMENTARY NOTES

12a DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13 ABSTRACT *(Maximum 200 words)*

This was a viewgraph presentation at the Government and Industry DMS Solutions Workshop. It explained the form, fit, function, and validation of the Generalized Emulation Microcircuit Program.

Published in *DMS Solutions Workshop Proceedings*.

14 SUBJECT TERMS			15 NUMBER OF PAGES
Electronic Devices, Components and Subsystems Microcircuits Emulation/Emulator		Diminishing Manufacturing Source	16 PRICE CODE
17 SECURITY CLASSIFICATION OF REPORT	18 SECURITY CLASSIFICATION OF THIS PAGE	19 SECURITY CLASSIFICATION OF ABSTRACT	20 LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAME AS REPORT

21a NAME OF RESPONSIBLE INDIVIDUAL	21b TELEPHONE *(Include Area Code)*	21c OFFICE SYMBOL
H. Hanson	(619) 553-2674	Code 552

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

HARVEY HANSON

NRaD

JOHN CHRISTENSEN

DLA

RESEARCH, DEVELOPMENT, TEST AND EVALUATION DIVISION
NAVAL COMMAND, CONTROL AND OCEAN SURVEILLANCE CENTER
SAN DIEGO, CA

HQ, DEFENSE LOGISTICS AGENCY
CAMERON STATION
ALEXANDRIA, VA

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

FORM, FIT, AND FUNCTION SPECIFICATIONS

COMBINATION OF:

ORIGINAL SPECIFICATION

MEASURED TYPICAL DEVICE CHARACTERIZATION

CHARACTERISTICS INHERENT TO ORIGINAL FABRICATION TECHNOLOGY

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

FLEXIBLE APPROACH:

- REDUCE NON RECURRING ENGINEERING
- MAINTAIN A SINGLE PROCESS SPANNING MULTIPLE FAMILIES
- PROGRAMMABLE TECHNOLOGY
- EXACT REPLACEMENT

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GATE ARRAY APPROACH

- GENERIC MACROCELLS: NOR, NAND, ETC.
  - REUSABILITY

BICMOS TECHNOLOGY

- MERGED BIPOLAR / CMOS PROCESS
  - BIPOLAR ELEMENTS IN I/O
  - CMOS FOR LOGIC FUNCTIONS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GATE ARRAY CONFIGURATIONS

ARRAY	I/O CELLS	CORE CELLS
GEM1218	48	1218
GEM384	26 + 2 POWER	384
GEM120	16 + 2 POWER	120
GEM 120-24	24 + 2 POWER	120

TAILORED TO FIT INTO ORIGINAL PACKAGES

CORE CELL CONSISTS OF MULTIPLE TRANSISTORS, CAPS. ETC.

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

DEVELOPMENT PHASE - KEY ELEMENTS

- DEVELOP BICMOS PROCESS AND DOCUMENTATION
- DEVELOP GEM DESIGN LIBRARY
- PROTOTYPE PARTS THAT SPAN OBSOLETE FAMILIES
- TESTING
- SUPPORT / INTERFACE STRUCTURE
- APPLICATION / INSERTION PARTS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM ROUGH SCREEN CRITERION - GEMABILITY

DIGITAL TECHNOLOGY

TECHNOLOGIES INCLUDE:

TTL, STTL, LSTTL, DTL, RTL, ECL,
CMOS, PMOS, NMOS

PIN COUNT <= 48

GATE COUNT <=1000

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

PROTOTYPE DEVICES	ORIGINAL DEVICE
54LS00	LS TTL NAND
54LS107	LS TTL JK FLIP FLOP
CS720J	DTL NAND
MC955L	DTL JK FLIP FLOP
SH2100	CURRENT DRIVER
F10125	ECL TO TTL TRANSLATOR
C4485	TTL ARITHMETIC LOGIC UNIT
MM5060	PMOS SHIFT REGISTER
MC358A	ECL JK FLIP FLOP
54S181	S TTL ARITHMETIC LOGIC UNIT
DS8642	QUAD TRANSMITTER/RECEIVER

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

PART NO.	ORGANIZATION
D3205	DESC ORDER
SW728-1P	DESC ORDER
SM-B-746395	ETDL/CECOM
SM-B-746396	ETDL/CECOM
SM-B-746131	ETDL/CECOM
AM2505/RM2505	CRANE
932046-501B SC15175FH-3	WR
932631-001B SC15180LH-3/MC2118	WR
8250	HILL/NUWES
54LS261	IBM
DS7836J	DESC DEMO
DS8642J	DESC DEMO
159202/SYC2534A/MIC2534/10197	NRaD/RAMP
A3012961-1/HC2135/9428-049	ETDL/SINCGARS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION

- ONE YEAR BASE PERIOD
- FOUR ONE YEAR OPTION PERIODS

TWO MAIN COMPONENTS

- BASE EFFORT (CORE)
  - ENHANCEMENTS, SUPPORT
- DELIVERY ORDER (IDIQ)
  - IC RELATED PRODUCTION / SERVICES

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION PHASE (CORE ELEMENTS)

- TECHNOLOGY ENHANCEMENTS
  - DESIGN (LIBRARY ELEMENTS, STRUCTURE)
  - PROCESS (YIELDS, PROCESS CONTROLS)
- TECHNOLOGY SUPPORT
  - GEM DESIGN
  - GEM LIBRARY

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION PHASE (CORE ELEMENTS)

BASE LEVEL OF FABRICATION

INFORMATIONAL BRIEFINGS

ANNUAL CONTRACT BRIEFINGS

APPLICATION PARTS

PROGRAM MANAGEMENT

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION - CURRENT EFFORTS

- SCHOTTKY ARRAY
- HIGH VOLATGE ARRAY
- PROCESS MODIFICATIONS TO IMPROVE RUGGEDNESS
- APPLICATION / INSERTION DEVICES

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION:

- MENU APPROACH
  - MIX AND MATCH WORK ELEMENTS
  - CUSTOM TAILORING OF DELIVERABLES
    - LINE ITEM
    - DATA DELIVERABLES
  - PORTIONS OF REPLACEMENT TASKS POSSIBLE

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION:

STANDARD PROTOTYPE PART

40 PARTS

10 - 12 WEEKS

DATA PACKAGE RECEIPT

SAMPLES (IF AVAILABLE)

MINIMAL CUSTOMER INPUT REQUIRED

'REGULAR ORDER'

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION - EXAMPLES OF TASKS (NON INCLUSIVE)

CHARACTERIZATION OF OBSOLETE PARTS

TURNKEY IC DESIGN

DESIGN OF IC ELEMENTS

DESIGN OF NEW ARRAYS

CELL DESIGN NOTEBOOKS

MODIFICATION / EXTENSION OF GEM PROCESS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

JOHN CHRISTENSEN, GEM PROGRAM MANAGER, (703) 274-6445

DSN: 284-6445

HARVEY HANSON, GEM TECHNICAL ADVISOR, (619) 553-2674

DSN: 553-2674

LLOYD PETERS, SRI PROGRAM MANAGER, (415) 859-3650

JIM CRABBE, SARNOFF PROGRAM MANAGER, (609) 734-3299

CHERYL MONTONEY, CONTRACTING OFFICER, (513) 296-6671

DSN: 9986-6671

SCOTT SAVORY, CONTRACT SPECIALIST, (513) 296-5344

DSN: 986-5344

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION - FUTURE PLANS

- SMALLER GEOMETRIC FEATURE SIZE
  - SPEED
  - COMPLEXITY
- VHDL CAPABILITY
- EXPANDED DESIGN CENTERS
- COST REDUCTION EFFORTS
- STREAMLINING RESPECIFICATION PROCEDURES

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION PHASE

KEY DELIVERY ORDER ELEMENTS:

MIPR TO DESC

SOW OR DESCRIPTION OF WORK

ASSISTANCE IS AVAILABLE / INTERACTIVE

WITHIN THE SCOPE OF THE EFFORT

ASSISTANCE / COORDINATION IS AVAILABLE